AMENDMENTS TO THE CLAIMS

The following is a complete, marked-up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern, the method comprising:

forming a gate insulating layer having an initial thickness on a silicon substrate;

depositing a metal gate material on the gate insulating layer, the metal gate material including at least one metal layer;

etching the metal gate material to form a metal gate pattern;

forming a capping layer on the metal gate pattern; and

selectively oxidizing at least a portion of the silicon substrate without substantially oxidizing the at least one metal layer and without substantially increasing the initial thickness of the gate insulating layer.

2. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

the metal gate material includes a polysilicon layer; and

selectively oxidizing at least a portion of the silicon substrate also oxides a portion of the polysilicon layer.

3. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

the gate insulating layer includes at least one insulating material layer selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, metal oxides and metal silicates.

4. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

the metal layer is selected from the group consisting of W, Ni, Co, TaN, Ru-Ta, TiN, Ni-Ti, Ti-Al-N, Zr, Hf, Ti, Ta, Mo, MoN, WN, Ta-Pt and Ta-Ti.

5. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

the metal gate pattern has a stacked structure selected from the group consisting of a metal/barrier metal/polysilicon/gate insulator stack, a metal/polysilicon/gate insulator stack, a metal/barrier metal/gate insulator stack and a metal/gate insulator stack.

6. (ORIGINAL) The method as claimed in claim 1, wherein:

the metal gate pattern is formed of a gate mask/tungsten/tungsten nitride/polysilicon/gate insulator stack.

7. (PREVIOUSLY PRESENTED) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

forming the capping layer includes:

forming a silicon oxide layer on a surface of the semiconductor substrate and a top surface and sidewalls of the metal gate pattern, the silicon oxide layer being formed under conditions such that the at least one metal layer remains substantially unoxidized.

8. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 7, wherein:

the silicon oxide layer included in the capping layer has a thickness of not more than about 500 Å.

9. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 7, wherein:

forming the silicon oxide layer includes:

loading the silicon substrate on which the metal gate pattern is formed into a reaction chamber;

injecting a nitrogen source gas into the reaction chamber, the conditions in the reaction chamber being sufficient to cause the nitrogen source gas to form a nitrogen atmosphere within the reaction chamber; and

injecting a silicon source gas and an oxygen source gas into the reaction chamber under conditions sufficient to cause the silicon oxide layer to form on the metal gate pattern.

10. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 9, wherein:

the nitrogen atmosphere is substantially free of oxygen.

11. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 10, wherein:

the nitrogen source gas includes ammonia.

12. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 9, wherein:

the silicon source gas includes at least one source gas selected from a group consisting of SiH_4, Si_2H_6, DCS, TCS and HCD; and

the oxygen source gas includes at least one source gas selected from a group consisting of N_2O, NO and O_2.

13. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 9, wherein:

the injection of the silicon source gas is initiated at a time no later than the injection of the oxygen source gas is initiated.

14. (PREVIOUSLY PRESENTED) A method of fabricating a semiconductor device having a metal gate pattern according to claim 9, wherein:

the injection of the nitrogen source gas into the reaction chamber is terminated under a condition selected from a group consisting of:

after the injection of the oxygen source gas has been initiated,

substantially simultaneously with the initiation of the oxygen source gas, and

before injection of the oxygen source gas or injection of the silicon source gas has been initiated.

15. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 9, wherein:

forming the silicon oxide layer includes a chemical vapor deposition process selected from a group consisting of plasma enhanced CVD, remote plasma enhanced CVD, high density plasma CVD, thermal CVD, laser CVD and hot filament CVD.

16. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 7, further comprising:

etching the silicon oxide layer to form silicon oxide spacers on the sidewalls of the metal gate pattern.

17. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 7, further comprising:

depositing a silicon nitride layer on the silicon oxide layer.

18. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 17, further comprising:

etching the silicon nitride layer to form silicon nitride spacers on the silicon oxide layer formed on the sidewalls of the metal gate pattern.

19. (PREVIOUSLY PRESENTED) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

forming the capping layer includes:

forming a silicon nitride layer on a portion of the surface of the semiconductor substrate and the top surface and sidewall of the metal gate pattern, the silicon nitride layer being formed under conditions such that the at least one metal layer remains substantially unoxidized.

20. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, wherein:

selectively oxidizing at least a portion of the silicon substrate without substantially oxidizing the at least one metal layer uses a wet oxidation process utilizing partial pressures of H_2O and H_2.

21. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 1, further comprising:

implanting impurity ions into the portion of the silicon substrate using the metal gate pattern as an ion implantation mask after the portion of the silicon substrate has been selectively oxidized.

22. (ORIGINAL) A method of fabricating a semiconductor device having a metal gate pattern according to claim 2, wherein:

the metal gate pattern has a width of not more than about 100 nm;

the capping layer has a thickness of not more than about 150 Å; and

the initial thickness of the gate insulating layer is increased by less than 10 Å.

23. (PREVIOUSLY PRESENTED) A semiconductor device comprising:

a semiconductor substrate;

a gate insulator formed on the semiconductor substrate; and

a metal gate pattern formed on the gate insulator; wherein

the metal gate pattern has a top surface and substantially vertical sidewalls and includes:

a first conductor pattern formed on the gate insulator, the first conductor pattern includes silicon and has a first oxidation rate;

a second conductor pattern formed on the first conductor pattern, the second conductor pattern includes a metal and has a second oxidation rate; and

a capping layer configured and arranged on the sidewalls of the metal gate pattern, whereby the first oxidation rate of the first conductor pattern is enhanced relative to the second oxidation rate of the second conductor pattern.

24. (ORIGINAL) A semiconductor device according to claim 23, wherein:

the first conductor pattern includes polysilicon; and

the second conductor pattern includes tungsten.

25. (ORIGINAL) A method of fabricating a semiconductor device according to claim 23, the method comprising:

forming a gate insulating layer on a silicon substrate;

forming a first conductive layer on the gate insulating layer;

forming a second conductive layer on the first conductor layer;

etching portions of the second conductive layer and the first conductive layer to form a metal gate pattern;

forming a capping layer on the metal gate pattern; and

selectively oxidizing the silicon substrate and the first conductive layer without substantially oxidizing the second conductive layer and without substantially increasing a thickness of the gate insulating layer.

26. (PREVIOUSLY PRESENTED) A method of fabricating a semiconductor device having a metal gate pattern, the method comprising:

forming a gate insulating layer having an initial thickness on a silicon substrate;

depositing a metal gate material on the gate insulating layer, the metal gate material including at least one metal layer;

etching the metal gate material to form a metal gate pattern;

forming a capping layer on the metal gate pattern; and

selectively oxidizing, with the capping layer present on top of the metal gate pattern, at least a portion of the silicon substrate without substantially oxidizing the at least one metal layer and without substantially increasing the initial thickness of the gate insulating layer.

27. (NEW) The semiconductor device according to claim 23, wherein the capping layer is a silicon oxide layer.